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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,359	12/14/2001	Michael Joachim Wolf	Q67426	1154
75	90 11/30/2005		EXAM	INER
SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC			JONES, PRENELL P	
2100 Pennsylva Washington, D	nia Avenue, N.W.		ART UNIT	PAPER NUMBER
washington, D	C 20037-3213		2668	
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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	B
Office Action Summan	10/014,359	WOLF ET AL.	1)-
Office Action Summary	Examiner	Art Unit	
	Prenell P. Jones	2667	
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence addr	ess -
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period w  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tin will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	N. nely filed the mailing date of this common (35 U.S.C. § 133).	
Status			
<ol> <li>Responsive to communication(s) filed on 14 December 2a)</li> <li>This action is FINAL. 2b)</li> <li>Since this application is in condition for allower closed in accordance with the practice under Exercise.</li> </ol>	action is non-final. nce except for formal matters, pro		nerits is
Disposition of Claims			
4) Claim(s) 1-15 is/are pending in the application.  4a) Of the above claim(s) is/are withdray  5) Claim(s) is/are allowed.  6) Claim(s) 1,3-8,10,11,14 and 15 is/are rejected.  7) Claim(s) 2,9,12 and 13 is/are objected to.  8) Claim(s) are subject to restriction and/or  Application Papers  9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acceed to the description of	vn from consideration.  r election requirement.  r.  epted or b) □ objected to by the Edrawing(s) be held in abeyance. See ion is required if the drawing(s) is objected.	e 37 CFR 1.85(a). ected to. See 37 CFR	
Priority under 35 U.S.C. § 119			
<ul> <li>12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents</li> <li>2. Certified copies of the priority documents</li> <li>3. Copies of the certified copies of the prior application from the International Bureau</li> <li>* See the attached detailed Office action for a list of the priorical strain of the certified copies of the priorical strain of the p</li></ul>	s have been received. s have been received in Application ity documents have been received (PCT Rule 17.2(a)).	on No ed in this National St	age
Attachment(s)    Notice of References Cited (PTO-892)   Notice of Draftsperson's Patent Drawing Review (PTO-948)   Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)   Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa	ite	52)

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#### Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 3, 5-8, 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

3. Regarding claims 5, Applicant is claiming in line 2-3, "the at least one first delayed

clock signal or the second delayed clock signal," which is unclear to Examiner as to exactly

what Applicant is claiming, because Applicant does not claim a first delayed clock signal or

second delayed clock signal in claim 1. Instead, Applicant claims a "first delay means",

"delaying the at least one first clock signal by a first delay time". Examiner questions is the

"at least one first delayed clock signal" the same as a "first delay time?" Also, is "at least one

second delayed clock signal" the same as a "second delay time? Claims 6 and 7 depend on

claim 5; therefore, claim 6 and 7 are rejected as well.

Regarding claim 8, Applicant is claiming in line 3-5, "the *first delayed clock signal* or

the second delayed clock signal," which is unclear to Examiner as to exactly what Applicant

is claiming, because Applicant does not claim a first delayed clock signal or second delayed

clock signal in claim 1.

Regarding claim 3, Applicant is claiming in line 2, "they delay," which is unclear to

Examiner exactly what Applicant is claiming. Examiner questions, who is "they"

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Regarding claim 10, Applicant is claiming in line 3, "they change," which is unclear to Examiner exactly what Applicant is claiming. Examiner questions, who is "they"

Regarding claim 11, Applicant is claiming in line 3, "they change," which is unclear to Examiner exactly what Applicant is claiming. Examiner questions, who is "they"

4. Claim 5 recites the limitation "the *at least one first delayed clock signal* or the *second delayed clock signal*" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Claims 6 and 7 depend on claim 5 therefore claim 6 and 7 are rejected as well.

### Claim Objections

5. Claim 14 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claims 1 and 12. See MPEP § 608.01(n). Accordingly, the claim 14 has not been further treated on the merits.

## Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

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evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamamoto et al (US PAT. 5,987,619) in view and Kazama et al (US PAT. 4,227,251).

Regarding claims 1 and 15, Hamamoto discloses phase compensation circuit/phase compensation module wherein the architecture includes determining time for delay, variable delay circuit and delay circuit (first delay means and second delay means) as associated with an internal clock signal and external clock signal (first clock/second clock), phase comparator/phase adjustment means (Abstract, Fig. 1, col. 2, line 26-40, col. 3, line 40 thru col. 4, line 65, col. 5, line 5-65). However, Hamamoto is silent on a first clock signal presented at the output of the end of the first delay. In a communication system phase compensation environment, Kazama discloses phase synchronizing clock pulses wherein the architecture includes a first/second delay circuits with associated clocks (first/second clock), clock pulses, delay time, counter is utilized as a phase detector at output of delay circuits for adjusting outputs (Fig. 4, col. 4, line 46 thru col. 5, line 67). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a phase adjusting means at the output of the first delay associated with a first clock signal as taught by the teachings of Kazama with the teachings of Hamamoto for the purpose of further minimizing and managing delay and optimize phase synchronization process.

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### Allowable Subject Matter

4. Claims 2, 9, 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Although the combined cited art discloses phase compensation associated in a telecommunication environment wherein utilization of a first/second delay unit along with corresponding first/second clock signals and associated delay time, and adjusting the phase, they fail to teach or suggest with respect to claim 2, the first delay time and/or a start value for the second delay time are predetermined as a function of a maximum expected phase difference between the at least one first clock signal and the second clock signal and/or as a function of a maximum expected propagation time difference, which is caused by the transmission paths of different lengths, with respect to claim 3, first delay time corresponds to a maximum expected phase difference and/or maximum expected propagation time difference between at least one first clock signal and the second clock signal, with respect to claim 9, the first or second start value is performed only upon attainment of a predetermined first deviation tolerance value, while the converse applies upon the attainment of a second deviation tolerance value which is smaller than the first deviation tolerance value, with respect to claim 12, control means on a console of a network device for transmission network with a synchronous digital hierarchy (SDH).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

November 25, 2005

CHIEH M. FAN SUPERVISORY PATENT EXAMINER

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